Data Sheet

Document # STNA504-M1

IceWings™ Product Datasheet (STNA504)

4x4 Multi-standard Low Power RF Transceiver

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DEVICE PRECAUTIONS

ESD Precaution

This is an ESD Sensitive Device manufactured in the CMOS process. It is therefore susceptible to damage from excessive voltage such as that caused by static discharge. Proper ESD precautions must be taken during handling, storage and operation of this device. ESD Specifications for this device are provided in the Systems Specifications section of the datasheet.

Moisture Sensitivity

Device is qualified to IPC/FJEDEC J-STD-020B, which determines moisture sensitivity and acceptable storage conditions. To avoid potential device damage, please ensure that this product is not exposed to any liquids, moisture, or high humidity environments. Devices are to be stored in sealed dry-packed bags.

Maximum Device Stresses

Stresses beyond those listed may cause permanent damage to the device or may impair device reliability. The device is to be operated solely within the minimum and maximum specifications outlined within this datasheet.

Contents

List of Figures

List of Tables

General Description

IceWings™ is an innovative RF transceiver with 4 integrated transmitters and receivers that supports a wide range of standards in signal frequencies below 7.2GHz and enables mmWave applications by intermediate to baseband conversion. This unique product with wide-band low noise amplifiers and one-of-a-kind multi-band capability offers the highest signal quality and the lowest power consumption in the industry. IceWings has applications in the 5G O-RAN infrastructure market targeting Radio Units (RU) as well as small cells and gNodeBs. IceWings is part of Arctic's suite of world's first multi-standard ultra-wide-band RF transceiver solutions specifically designed to facilitate the virtualization of cellular ecosystem and disaggregation of hardware and software in 5G networks. These products are derived from a unique, patented high speed and ultra-wide-band RF/Mixed mode technology used in multiple generations of Arctic's products currently in deployments.

Benefits

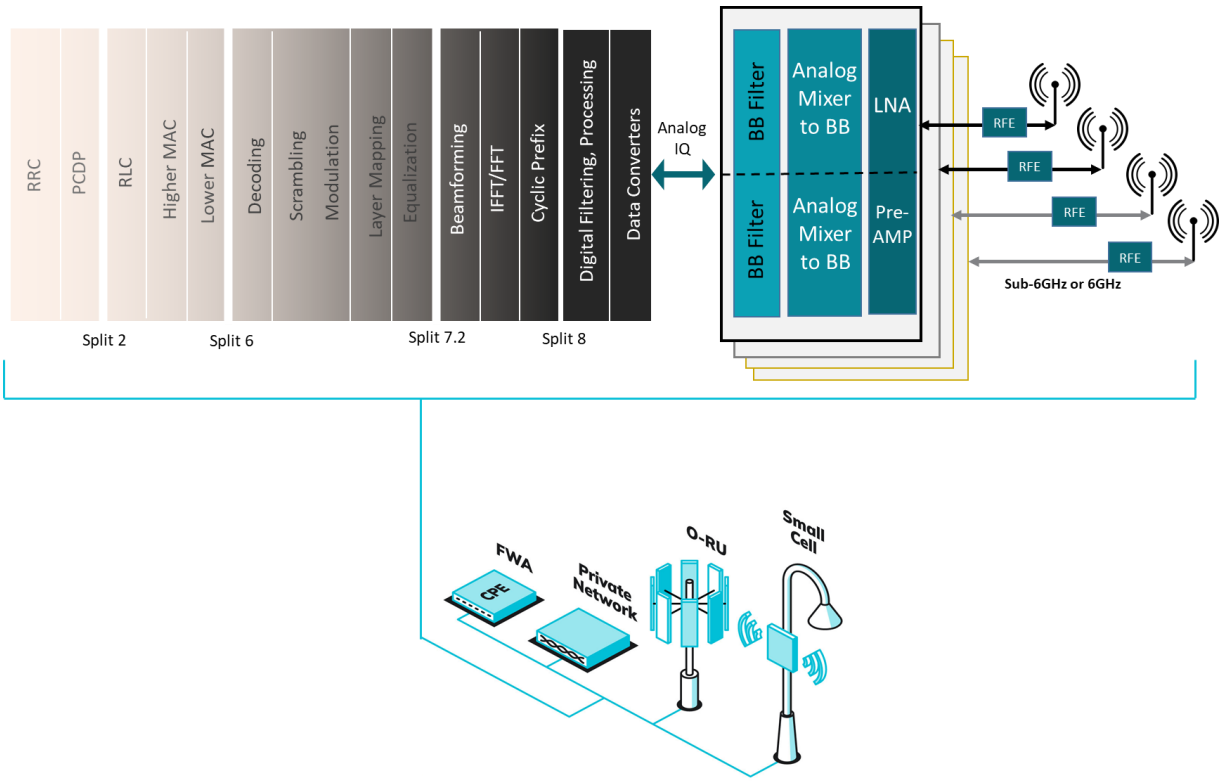
- **Lower power consumption:** Accelerate the deployment of 5G by offering new technology perfect for reducing overall power consumption of the Radio Unit (RU) or Distributed Radio Unit (dRU)
- **Multi-standard interface:** Support for a wide range of wireless standards with a flexible scalable interface design.
- **High-performance solutions:** Complying with 5G NR, WiFi, WiFi 6/7 and 4G LTE specifications and offering superior performance when it comes to signal quality, noise, linearity, and power consumption due to their inherently innovative architecture.
- **Scalable support**: Supports various 5G applications including gNodeB, private networks, Enterprises, IoT, and Small Cells.

Features

- Quad Tx/Rx, Analog RF technology
- 4 Wide-band single-ended RF inputs covering RF ranges of 600MHz to 7.2GHz
    - Port 1: 600MHz-965MHz
    - Port 2: 1400MHz-2700MHz
    - Port 3: 3300MHz-5200MHz
    - Port 4: 5000MHz-7125MHz
- Reduces the number of RF switches in multi band designs
- Integrated LNA and PA Pre-amp
- FR1 support: 5/10/15/20/40/50/60/80/100/160/200/300/400 MHz Channel BW
- FR2 support: 400MHz, IF frequency 3.3GHz-7.12GHz
- Analog IQ interface with Baseband SoC
- Wide Band 4 RX paths can be used for DPD observation paths reducing complexity in TDD modes
- Integrated 2 Low phase noise fractional synthesizers supporting TDD, FDD and two 2x2 in TDD
- Sub-1W Power consumption for TDD 4x4 Transceiver
- IceWings can also support 400MHz bandwidth for mmWave applications.

Use Case

Sub_6GHz and 6GHz Analog Interface Use Case



1 Functional Block Diagram

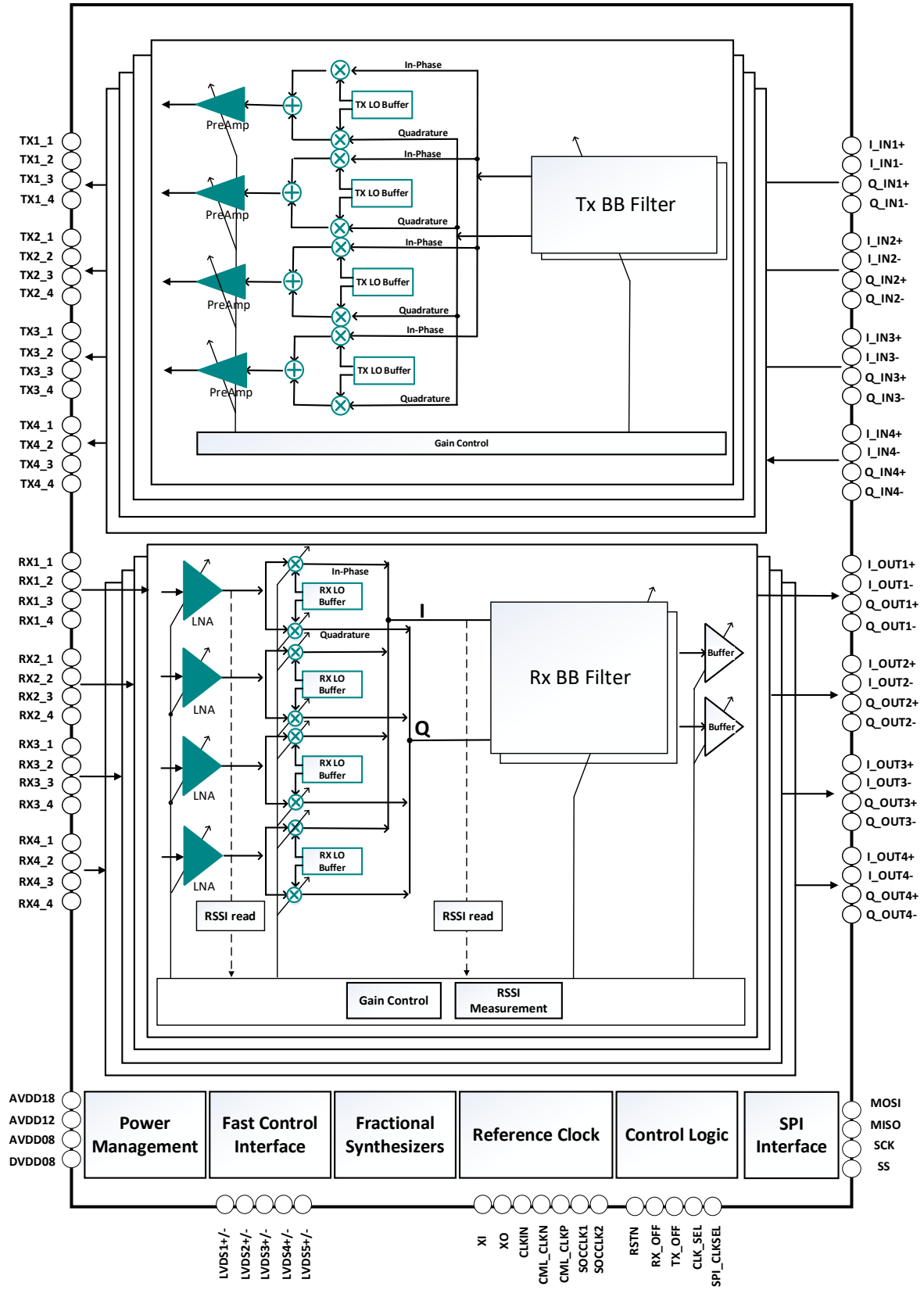


Figure 1-1-1 4x4 IceWings Functional Block Diagram

2 IceWings Spec

2.1 General Specification

- Analog IQ interface to the Baseband
- Compliant with 3GPP LTE/NR release 15 and 16 specifications
- Compliant with WiFi 802.11ax, 802.11a, 802.11b/g,802.11ac/n, 802.11d, 802.11e, WiFi – 6 specifications including LVDS gain control support
- Compliant with 5G NR mmWave specifications for IF to IQ down/up conversion
- Modes
  - TDD modes for NR/WiFi.
  - FDD for LTE
- Supported frequency bands:
  - 0.6 GHz to 7.25 GHz
  - RF ports (total 4) and frequency band support
    - Port 1: 600MHz-965MHz
    - Port 2: 1400MHz-2700MHz
    - Port 3: 3300MHz-5200MHz
    - Port 4: 5000MHz-7125MHz
- Channel Bandwidth (supported on each RF port and TX/RX chain)
  - 5/10/15/20/40/50/60/80/100/160/200/300/400 MHz Channel BW selection
- DPD
  - Wide BW (up to 400MHz) Tx and Rx support enabling digital linearization at the SoC
- Supports Dual 2x2 or Single 4x4 Configuration.
- Each of 4x4 is a Quad-band input (LB/MB/MHB/HB)
- Support for mechanism to sync the LO of one IceWings chip to the other for at least 2 chips (8x8)
- Each TX and RX path independently turn off to save power
- RF port impedance (single ended) = 50 Ohms
- Operating temperature -40C to +85C
- Receive mode (1,2,3 or 4 receivers active)
- Transmit mode (1, 2,3 or 4 transmitters active)
- Power Consumption:

Table 2-1 Power consumption

BW	*Mode TDD/FDD*	*Power consumption*
Low BW (20MHz)	*FDD*	*1230 mW*
Mid BW (200 MHz)	*FDD*	*1350 mW*
Mid BW (200MHz)	*TDD (50-50)*	*875 mW*
Mid BW (200MHz)	*TDD (80-20)*	*800mW*
High BW (400MHz)	*TDD (50-50)*	*1020 mW*

Table 2-2 Current consumption

Current Consumption when RxTx on	Maximum	Unit
V2P0	100	mA
V1P8	350	mA
V1P45	100	mA
V1P2	400	mA
V0P9	200	mA

2.2 Transmitter

- Transmit Signal Level
  - -10dBm average output power

Table 2-3 Transmitter Specifications

	Min	Typ	Max
ACLR @100MHz and -10dBm average output power (PAR <10)			
600MHz		-46 dBc	
1800MHz		-46 dBc	
2600MHz		-46 dBc	
3800MHz		-46 dBc	
4800MHz		-46 dBc	
5700MHz		-45 dBc	
7200MHz		-45 dBc	
EVM (After IQ Imbalance Correction)			
600MHz			1.55%
1800MHz			1.85%
2600MHz			1.95%
3800MHz			2.00%
4800MHz			2.55%
5700MHz			2.63%
7200MHz			2.75%
Unwanted Emissions above 1 GHz **Test Conditions:** **Resolution Bandwidth = 1 MHz RMS** **Power = -1 dBm OFDM Signal** **RF Channel BW** **(10/15/20/40/50/60/80/100/160 MHz)**		-75 dBm	
IQ Imbalance Correction		IceWings has special Calibration technique that will assist IQ Imbalance correction at the Digital side	

2.3 Receiver

Table 2-4 Receiver Specifications

	Min	Typ	Max
Gain Range **BB 30 dB (2dB steps)** **LNA 42 dB (6dB steps)**	-4dB		68 dB
Gain Step		2 dB	
Gain Accuracy		+/- 1dB	
RF Gain Flatness (PVT)	- 2 dB		+2 dB
Rx Gain Control Latency **(After the IceWings register write to RF gain settled**		▪ Total BW=400MHz: 65ns (Filter is 35ns) ▪ Total BW=200MHz: 100ns (Filter is 70ns) ▪ Total BW= 40MHz: 250ns (Filter is 200ns)	
Rx gain variation (PVT)	-2.5dB		+2.5dB
Receive Optimum Output Voltage **Common Mode** **Peak to Peak Differential Voltage**		0.8V 0.8V	
BB DAC Interface Common Mode Voltage		Interface to current Mode DAC with a resistor on Board.	
Receive Analog Signal Path Delay		▪ For BW=400MHz (Filter 200MHz) Delay=4ns ▪ For BW=300MHz (Filter 150MHz) Delay=5ns ▪ For BW=200MHz (Filter 100MHz) Delay=7ns ▪ For BW=160MHz (Filter 80 MHz) Delay= 9ns ▪ For BW=100MHz (Filter 50 MHz) Delay= 14ns ▪ For BW=40MHz (Filter 20 MHz) Delay= 35ns ▪ For BW=20MHz (Filter 10 MHz) Delay= 70ns ▪ For BW= 10MHz (Filter 5 MHz) Delay= 140ns	
Receive Inter-RF Path Isolation RXi to RXj		50dB	
Receive BB filter passband ripple		0.5dB	

Receive Baseband Filter	Filter 5/10/15/20/40/50/60/80/100/160/200/300/400 MHz Channel BW selection		
Receive Baseband Filter Rejection **Adjacent Channel Rejection f= fc +- B** **Alternate Channel Rejection f= fc +-2B** **Where,** **B = RF Channel Bandwidth (10/20/25/30/40/50/60/80/100/160 MHz)**	8.5dB 46dB		
NF at max Gain	3dB		5.5dB
Rx Baseband Filter Group Delay Variation **(ΔTg(f)*B)** **F < 0.3*B** **0.3*B < f < 0.46*B** **Where, ΔTg(f)=Deviation of group delay at frequency, f, relative to DC,** **B = RF Channel BW (10/15/20/40/50/60/80/100/160/200/300/400MHz)**	-0.35 -0.80		+0.35 +0.80
Receive Baseband Filter Corner (Fcnr/RF Channel BW) **Fcnr = Filter corner frequency**		0.625	
IIP3		6dBm	
Receive path EVM @100MHz CH BW @PIN -20dBm (After IQ Imbalance Correction)			
600MHz		1.50%	
1800MHz		1.80%	
2600MHz		1.85%	
3800MHz		2.00%	
4800MHz		2.45%	
5700MHz		2.55%	
7200MHz		2.65%	

2.3.1 Gain

IceWings supports 3 stage gain control: RF, Mixer and BB gain provided by Baseband IC.

2.4 Calibration

- DC Offset correction
- IQ Mismatch Calibration support to the BB Chip
- Loop back Support for calibration

2.5 Integrated Multi-band LNA

2.6 Digital Interface

- SPI @ 50 MHz for Register programming
- LVDS digital interface for reading RSSI for every RX and writing Gain
- Reset Pin
- RSSI measurement for each RX Channel
- Max DL modulation: 1024 QAM
- Max UL modulation: 256 QAM
- Component carrier bandwidth: 10, 20, 40, 50, 60, 80, 100
- IBW support: Up to 400MHz

2.7 Bands

Table 2-5 Supported Frequency Bands

NR *operating band*	Uplink (UL) *operating band* BS receive / UE transmit $F_{UL,low}$ – $F_{UL,high}$	Downlink (DL) *operating band* BS transmit / UE receive $F_{DL,low}$ – $F_{DL,high}$	Duplex Mode	
n1	1920 MHz – 1980 MHz	2110 MHz – 2170 MHz	FDD	port 2
n2	1850 MHz – 1910 MHz	1930 MHz – 1990 MHz	FDD	port 2
n3	1710 MHz – 1785 MHz	1805 MHz – 1880 MHz	FDD	port 2
n5	824 MHz – 849 MHz	869 MHz – 894 MHz	FDD	port 1
n7	2500 MHz – 2570 MHz	2620 MHz – 2690 MHz	FDD	port 2
n8	880 MHz – 915 MHz	925 MHz – 960 MHz	FDD	port 1
n12	699 MHz – 716 MHz	729 MHz – 746 MHz	FDD	port 1
n20	832 MHz – 862 MHz	791 MHz – 821 MHz	FDD	port 1
n25	1850 MHz – 1915 MHz	1930 MHz – 1995 MHz	FDD	port 2
n28	703 MHz – 748 MHz	758 MHz – 803 MHz	FDD	port 1
n34	2010 MHz – 2025 MHz	2010 MHz – 2025 MHz	TDD	port 2
n38	2570 MHz – 2620 MHz	2570 MHz – 2620 MHz	TDD	port 2
n39	1880 MHz – 1920 MHz	1880 MHz – 1920 MHz	TDD	port 2
n40	2300 MHz – 2400 MHz	2300 MHz – 2400 MHz	TDD	port 2
n41	2496 MHz – 2690 MHz	2496 MHz – 2690 MHz	TDD	port 2
n50	1432 MHz – 1517 MHz	1432 MHz – 1517 MHz	TDD	port 2

n51	1427 MHz – 1432 MHz	1427 MHz – 1432 MHz	TDD	port 2
n66	1710 MHz – 1780 MHz	2110 MHz – 2200 MHz	FDD	port 2
n70	1695 MHz – 1710 MHz	1995 MHz – 2020 MHz	FDD	port 2
n71	663 MHz – 698 MHz	617 MHz – 652 MHz	FDD	port 1
n74	1427 MHz – 1470 MHz	1475 MHz – 1518 MHz	FDD	port 2
n75	N/A	1432 MHz – 1517 MHz	SDL	port 2
n76	N/A	1427 MHz – 1432 MHz	SDL	port 2
n77	3300 MHz – 4200 MHz	3300 MHz – 4200 MHz	TDD	port 3
n78	3300 MHz – 3800 MHz	3300 MHz – 3800 MHz	TDD	port 3
n79	4400 MHz – 5000 MHz	4400 MHz – 5000 MHz	TDD	port 3
n80	1710 MHz – 1785 MHz	N/A	SUL	port 2
n81	880 MHz – 915 MHz	N/A	SUL	port 1
n82	832 MHz – 862 MHz	N/A	SUL	port 1
n83	703 MHz – 748 MHz	N/A	SUL	port 1
n84	1920 MHz – 1980 MHz	N/A	SUL	port 2
n86	1710 MHz – 1780 MHz	N/A	SUL	port 2

E-UTRA Operating Band	**Uplink (UL) operating band** **BS receive** **UE transmit** F_{UL_low} – F_{UL_high}	**Downlink (DL) operating band** **BS transmit** **UE receive** F_{DL_low} – F_{DL_high}	**Duplex Mode**	
1	1920 MHz – 1980 MHz	2110 MHz – 2170 MHz	FDD	port 2
2	1850 MHz – 1910 MHz	1930 MHz – 1990 MHz	FDD	port 2
3	1710 MHz – 1785 MHz	1805 MHz – 1880 MHz	FDD	port 2
4	1710 MHz – 1755 MHz	2110 MHz – 2155 MHz	FDD	port 2
5	824 MHz – 849 MHz	869 MHz – 894MHz	FDD	port 1
7	2500 MHz – 2570 MHz	2620 MHz – 2690 MHz	FDD	port 2
8	880 MHz – 915 MHz	925 MHz – 960 MHz	FDD	port 1
9	1749.9 MHz – 1784.9 MHz	1844.9 MHz – 1879.9 MHz	FDD	port 2
10	1710 MHz – 1770 MHz	2110 MHz – 2170 MHz	FDD	port 2
11	1427.9 MHz – 1447.9 MHz	1475.9 MHz – 1495.9 MHz	FDD	port 2
12	699 MHz – 716 MHz	729 MHz – 746 MHz	FDD	port 1
13	777 MHz – 787 MHz	746 MHz – 756 MHz	FDD	port 1
14	788 MHz – 798 MHz	758 MHz – 768 MHz	FDD	port 1
17	704 MHz – 716 MHz	734 MHz – 746 MHz	FDD	port 1
18	815 MHz – 830 MHz	860 MHz – 875 MHz	FDD	port 1
19	830 MHz – 845 MHz	875 MHz – 890 MHz	FDD	port 1
20	832 MHz – 862 MHz	791 MHz – 821 MHz	FDD	port 1
21	1447.9 MHz – 1462.9 MHz	1495.9 MHz – 1510.9 MHz	FDD	port 2
22	3410 MHz – 3490 MHz	3510 MHz – 3590 MHz	FDD	port 3
231	2000 MHz – 2020 MHz	2180 MHz – 2200 MHz	FDD	port2

24	1626.5 MHz	–	1660.5 MHz	1525 MHz	–	1559 MHz	FDD	port 2
25	1850 MHz	–	1915 MHz	1930 MHz	–	1995 MHz	FDD	port 2
26	814 MHz	–	849 MHz	859 MHz	–	894 MHz	FDD	port 1
27	807 MHz	–	824 MHz	852 MHz	–	869 MHz	FDD	port 1
28	703 MHz	–	748 MHz	758 MHz	–	803 MHz	FDD	port 1
29	N/A			717 MHz	–	728 MHz	FDD (NOTE 2)	port 1
30	2305 MHz	–	2315 MHz	2350 MHz	–	2360 MHz	FDD	port 2
32	N/A			1452 MHz	–	1496 MHz	FDD (NOTE 2)	port 2
33	1900 MHz	–	1920 MHz	1900 MHz	–	1920 MHz	TDD	port 2
34	2010 MHz	–	2025 MHz	2010 MHz	–	2025 MHz	TDD	port 2
35	1850 MHz	–	1910 MHz	1850 MHz	–	1910 MHz	TDD	port 2
36	1930 MHz	–	1990 MHz	1930 MHz	–	1990 MHz	TDD	port 2
37	1910 MHz	–	1930 MHz	1910 MHz	–	1930 MHz	TDD	port 2
38	2570 MHz	–	2620 MHz	2570 MHz	–	2620 MHz	TDD	port 2
39	1880 MHz	–	1920 MHz	1880 MHz	–	1920 MHz	TDD	port 2
40	2300 MHz	–	2400 MHz	2300 MHz	–	2400 MHz	TDD	port 2
41	2496 MHz	–	2690 MHz	2496 MHz	–	2690 MHz	TDD	port 2
42	3400 MHz	–	3600 MHz	3400 MHz	–	3600 MHz	TDD	port 3
43	3600 MHz	–	3800 MHz	3600 MHz	–	3800 MHz	TDD	port 3
44	703 MHz	–	803 MHz	703 MHz	–	803 MHz	TDD	port 1
45	1447 MHz	–	1467 MHz	1447 MHz	–	1467 MHz	TDD	port 2
46	5150 MHz	–	5925 MHz	5150 MHz	–	5925 MHz	TDD (NOTE 3, NOTE 4)	port 2
47	5855 MHz	–	5925 MHz	5855 MHz	–	5925 MHz	TDD	port 4
48	3550 MHz	–	3700 MHz	3550 MHz	–	3700 MHz	TDD	port 3
49	3550 MHz – 3700 MHz			3550 MHz – 3700 MHz			TDD (NOTE 8)	port 3
50	1432 MHz	-	1517 MHz	1432 MHz	-	1517 MHz	TDD	port 2
51	1427 MHz	-	1432 MHz	1427 MHz	-	1432 MHz	TDD	port 2
52	3300 MHz	-	3400 MHz	3300 MHz	-	3400 MHz	TDD	port 3
65	1920 MHz	–	2010 MHz	2110 MHz	–	2200 MHz	FDD	port 2
66	1710 MHz	–	1780 MHz	2110 MHz	–	2200 MHz	FDD (NOTE 5)	port 2
67	N/A			738 MHz	–	758 MHz	FDD (NOTE 2)	port 1
68	698 MHz	–	728 MHz	753 MHz	–	783 MHz	FDD	port 1
69	N/A			2570 MHz	–	2620 MHz	FDD (NOTE 2)	port 2
70	1695 MHz	–	1710 MHz	1995 MHz	–	2020 MHz	FDD[6]	port 2
71	663 MHz	–	698 MHz	617 MHz	–	652 MHz	FDD	port 1

74	1427 MHz – 1470 MHz	1475 MHz – 1518 MHz	FDD	port 2
75	N/A	1432 MHz – 1517 MHz	FDD (NOTE 2)	port 2
76	N/A	1427 MHz – 1432 MHz	FDD (NOTE 2)	port 2
85	698 MHz – 716 MHz	728 MHz – 746 MHz	FDD	port 1

WiFi *operating band*	**BW [MHz]**	**Freq [GHz]**	
2.4 GHz	20, 40, 80160	2.401 - 2.495	port 2
5 GHz	20, 40,80, 160	5.03 - 5.9	port 4
U-NII-5/6/7/8	20, 40, 80, 160	5.925-7.125	port 4

3 Architecture

3.1 4x Receivers

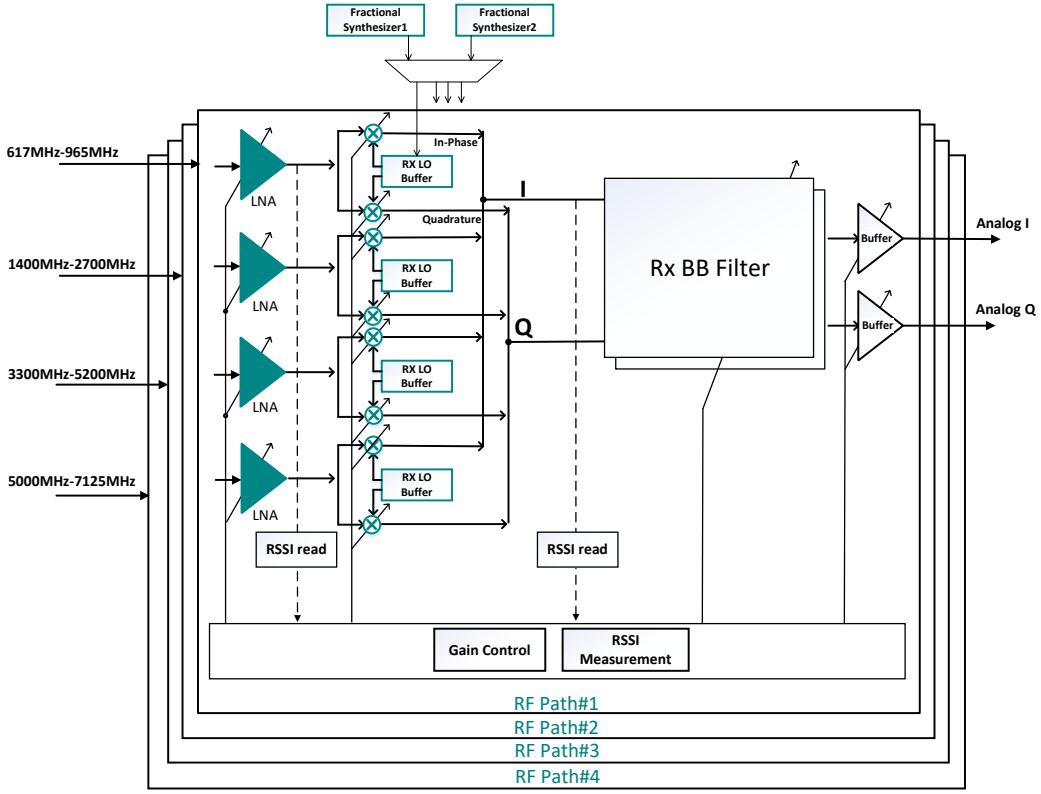


Figure 3-1 Receiver Architecture

3.2 4x Transmitters

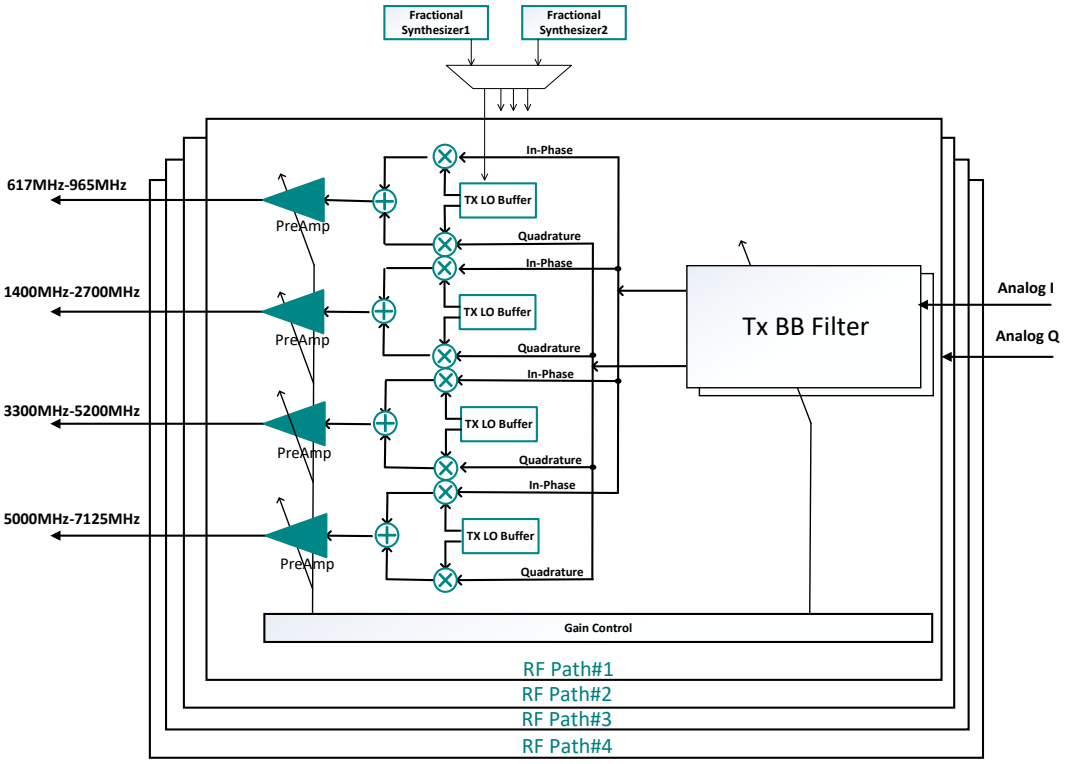


Figure 3-2 Transmitter Architecture

4 Pin Information

4.1 Pin Layouts

4.1.1 IceWings 156-Pin QFN Layout

Figure 5-1 shows the IceWings 156-pin layout. Table 5-1 lists the corresponding pin descriptions.

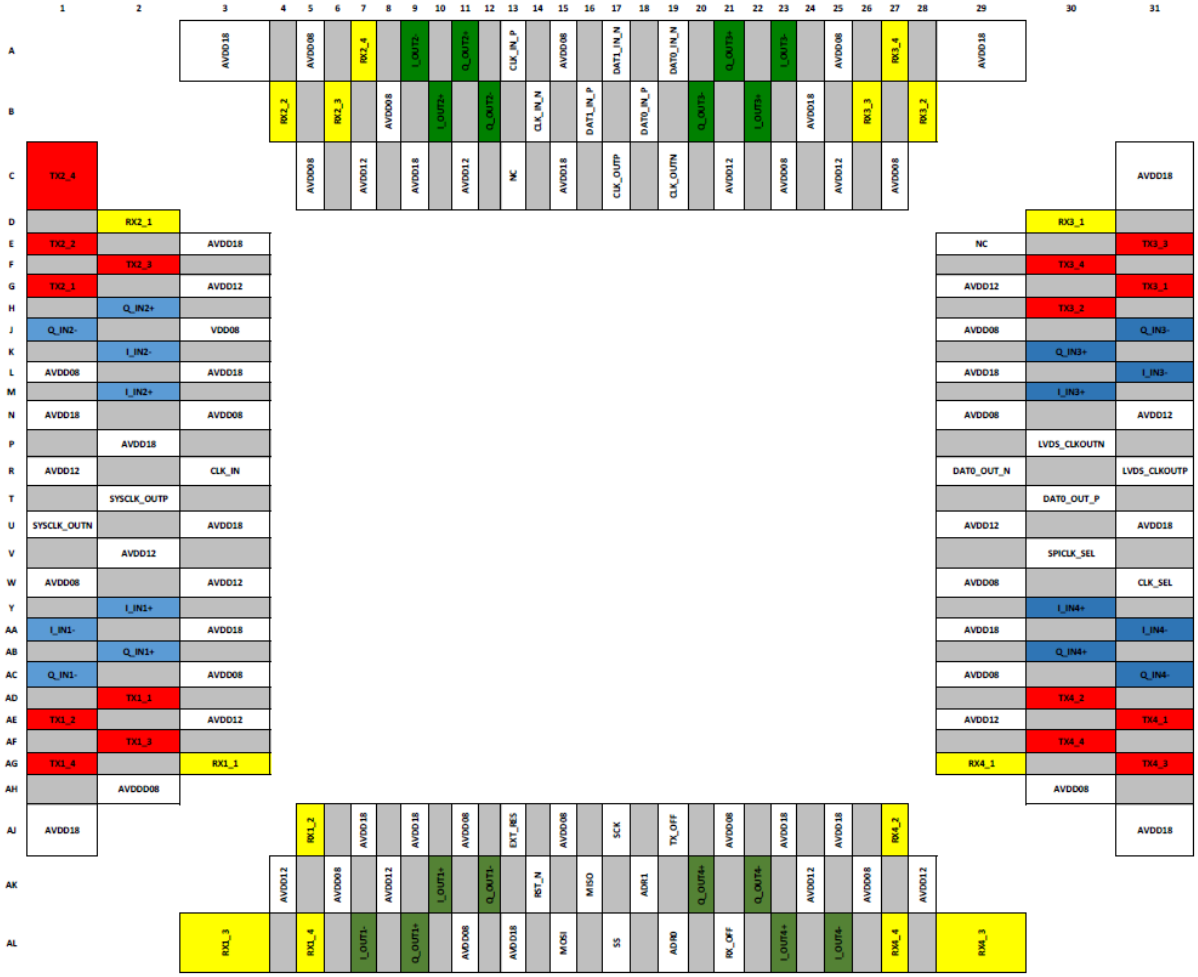


Figure 4-1 IceWings 156-Pin QFN Package Layout

4.1.2 IceWings 156-Pin QFN Descriptions

Table 4-1 IceWings 156-Pin QFN Descriptions

Pin ID	Pin Name	Type	Description
E3	AVDD18	Power 1.8 V	analog power 1.8v
G3	AVDD12	Power 1.2 V	analog power 1.2v
C1	TX2_4	Analog IO	RF output 7G (channel 2)
F2	TX2_3	Analog IO	RF output 5G (channel 2)
J3	VDD08	Power 0.8 V	analog power 0.8v
E1	TX2_2	Analog IO	RF output 3G (channel 2)
G1	TX2_1	Analog IO	RF output 1G (channel 2)
L3	AVDD18	Power 1.8 V	analog power 1.8v
H2	Q_IN2+	Analog IO	analog input+ IF_Q (channel 2)
J1	Q_IN2-	Analog IO	analog input- IF_Q (channel 2)
M2	I_IN2+	Analog IO	analog input+ IF_I (channel 2)
K2	I_IN2-	Analog IO	analog input- IF_I (channel 2)
L1	AVDD08	Power 0.8 V	analog power 0.8v
N3	AVDD08	Power 0.8 V	analog power 0.8v
N1	AVDD18	Power 1.8 V	analog power 1.8v
P2	AVDD18	Power 1.8 V	analog power 1.8v
R1	AVDD12	Power 1.2 V	analog power 1.2v
R3	CLK_IN	Digital IO	clock input
U1	SYSCLK_OUTN	CML IO	Clock output
T2	SYSCLK_OUTP	CML IO	Clock output
U3	AVDD18	Power 1.8 V	analog power 1.8v
V2	AVDD12	Power 1.2 V	analog power 1.2v
W3	AVDD12	Power 1.2 V	analog power 1.2v
W1	AVDD08	Power 0.8 V	analog power 0.8v
AA1	I_IN1-	Analog IO	analog input- IF_I (channel 1)
Y2	I_IN1+	Analog IO	analog input+ IF_I (channel 1)
AB2	Q_IN1+	Analog IO	analog input+ IF_Q (channel 1)
AC1	Q_IN1-	Analog IO	analog input- IF_Q (channel 1)
AA3	AVDD18	Power 1.8 V	analog power 1.8v
AD2	TX1_1	Analog IO	RF output 1G (channel 1)
AE1	TX1_2	Analog IO	RF output 3G (channel 1)
AC3	AVDD08	Power 0.8 V	analog power 0.8v
AF2	TX1_3	Analog IO	RF output 5G (channel 1)
AG1	TX1_4	Analog IO	RF output 7G (channel 1)
AE3	AVDD12	Power 1.2 V	analog power 1.2v
AJ1	AVDD18	Power 1.8 V	analog power 1.8v
AG3	RX1_1	Analog IO	RF input 1G (channel 1)
AH2	AVDD08	Power 0.8 V	analog power 0.8v
AJ5	RX1_2	Analog IO	RF input 3G (channel 1)
AK4	AVDD12	Power 1.2 V	analog power 1.2v

AJ7	AVDD18	Power 1.8V	analog power 1.8v
AL3	RX1_3	Analog IO	RF input 5G (channel 1)
AK6	AVDD08	Power 0.8 V	analog power 0.8v
AL5	RX1_4	Analog IO	RF input 7G (channel 1)
AJ9	AVDD18	Power 1.8 V	analog power 1.8v
AJ11	AVDD08	Power 0.8 V	analog power 0.8v
AK8	AVDD12	Power 1.2 V	analog power 1.2v
AK10	I_OUT1+	Analog IO	analog output+ IF_I (channel 1)
AL7	I_OUT1-	Analog IO	analog output- IF_I (channel 1)
AK12	Q_OUT1-	Analog IO	analog output- IF_Q (channel 1)
AL9	Q_OUT1+	Analog IO	analog output+ IF_Q (channel 1)
AL11	AVDD08	Power 0.8 V	analog power 0.8v
AJ13	EXT_RES	Analog IO	analog I/o – connected to external resistor
AL13	AVDD18	Power 1.8 V	analog power 1.8v
AJ15	AVDD08	Power 0.8 V	analog power 0.8v
AK14	RST_N	Digital IO	reset pin
AK16	MISO	Digital IO	MISO pin – SPI interface
AL15	MOSI	Digital IO	MOSI pin – SPI interface
AJ17	SCK	Digital IO	SCK pin – SPI interface
AL17	SS	Digital IO	SS pin – SPI interface
AK18	ADR1	Digital IO	Digital input – Chip Select
AL19	ADR0	Digital IO	Digital input – Chip Select
AJ19	TX_OFF	Digital IO	TX ON/OFF pin
AL21	RX_OFF	Digital IO	RX ON/OFF pin
AK20	Q_OUT4+	Analog IO	analog output+ IF_Q (channel 4)
AK22	Q_OUT4-	Analog IO	analog output- IF_Q (channel 4)
AL25	I_OUT4-	Analog IO	analog output- IF_I (channel 4)
AL23	I_OUT4+	Analog IO	analog output+ IF_I (channel 4)
AK24	AVDD12	Power 1.2 V	analog power 1.2v
AJ21	AVDD08	Power 0.8 V	analog power 0.8v
AJ23	AVDD18	Power 1.8 V	analog power 1.8v
AL27	RX4_4	Analog IO	RF input 7G (channel 4)
AK26	AVDD08	Power 0.8 V	analog power 0.8v
AL29	RX4_3	Analog IO	RF input 5G (channel 4)
AJ25	AVDD18	Power 1.8 V	analog power 1.8v
AK28	AVDD12	Power 1.2 V	analog power 1.2v
AJ27	RX4_2	Analog IO	RF input 3G (channel 4)
AH30	AVDD08	Power 0.8 V	analog power 0.8v
AG29	RX4_1	Analog IO	RF input 1G (channel 4)
AJ31	AVDD18	Power 1.8 V	analog power 1.8v
AE29	AVDD12	Power 1.2 V	analog power 1.2v
AF30	TX4_4	Analog IO	RF output 7G (channel 4)

AG31	TX4_3	Analog IO	RF output 5G (channel 4)
AC29	AVDD08	Power 0.8 V	analog power 0.8v
AD30	TX4_2	Analog IO	RF output 3G (channel 4)
AE31	TX4_1	Analog IO	RF output 1G (channel 4)
AA29	AVDD18	Power 1.8 V	analog power 1.8v
AB30	Q_IN4+	Analog IO	analog input+ IF_Q (channel 4)
AC31	Q_IN4-	Analog IO	analog input- IF_Q (channel 4)
Y30	I_IN4+	Analog IO	analog input+ IF_I (channel 4)
AA31	I_IN4-	Analog IO	analog input- IF_I (channel 4)
W29	AVDD08	Power 0.8 V	analog power 0.8v
V30	SPICLK_SEL	Digital IO	digital input pad - SPI clock mode (400k mode)
W31	CLK_SEL	Digital IO	digital input pad - chip clock mode (select between Xtal/external Osc)
U29	AVDD12	Power 1.2 V	analog power 1.2v
U31	AVDD18	Power 1.8 V	analog power 1.8v
R29	DAT0_OUT_N	Analog IO	analog IO - RF gain - data
T30	DAT0_OUT_P	Analog IO	analog IO - RF gain - data
P30	LVDS_CLKOUTN	Analog IO	analog IO - RF gain - clock
R31	LVDS_CLKOUTP	Analog IO	analog IO - RF gain - clock
N31	AVDD12	Power 1.2 V	analog power 1.2v
N29	AVDD08	Power 0.8 V	analog power 0.8v
L31	I_IN3-	Analog IO	analog input- IF_I (channel 3)
M30	I_IN3+	Analog IO	analog input+ IF_I (channel 3)
K30	Q_IN3+	Analog IO	analog input+ IF_Q (channel 3)
J31	Q_IN3-	Analog IO	analog input- IF_Q (channel 3)
L29	AVDD18	Power 1.8 V	analog power 1.8v
G31	TX3_1	Analog IO	RF output 1G (channel 3)
H30	TX3_2	Analog IO	RF output 3G (channel 3)
J29	AVDD08	Power 0.8 V	analog power 0.8v
E31	TX3_3	Analog IO	RF output 5G (channel 3)
F30	TX3_4	Analog IO	RF output 7G (channel 3)
G29	AVDD12	Power 1.2 V	analog power 1.2v
C31	AVDD18	Power 1.8 V	analog power 1.8v
D30	RX3_1	Analog IO	RF input 1G (channel 3)
C27	AVDD08	Power 0.8 V	analog power 0.8v
B28	RX3_2	Analog IO	RF input 3G (channel 3)
A29	AVDD18	Power 1.8 V	analog power 1.8v
C25	AVDD12	Power 1.2 V	analog power 1.2v
B26	RX3_3	Analog IO	RF input 5G (channel 3)
C23	AVDD08	Power 0.8 V	analog power 0.8v

A27	RX3_4	Analog IO	RF input 7G (channel 3)
B24	AVDD18	Power 1.8 V	analog power 1.8v
A25	AVDD08	Power 0.8 V	analog power 0.8v
C21	AVDD12	Power 1.2 V	analog power 1.2v
B22	I_OUT3+	Analog IO	analog output+ IF_I (channel 3)
A23	I_OUT3-	Analog IO	analog output- IF_I (channel 3)
B20	Q_OUT3-	Analog IO	analog output- IF_Q (channel 3)
A21	Q_OUT3+	Analog IO	analog output+ IF_Q (channel 3)
C19	CLK_OUTN	Digital IO	CMOS Clock
C17	CLK_OUTP	Digital IO	CMOS Clock
A19	DAT0_IN_N	Analog IO	analog IO - data 0 RF RSSI
B18	DAT0_IN_P	Analog IO	analog IO - data 0 RF RSSI
A17	DAT1_IN_N	Analog IO	analog IO - data 1 RF RSSI
B16	DAT1_IN_P	Analog IO	analog IO - data 1 RF RSSI
A15	AVDD08	Power 0.8 V	analog power 0.8v
C15	AVDD18	Power 1.8 V	analog power 1.8v
A13	CLK_IN_P	Analog IO	analog IO - clock RF RSSI
B14	CLK_IN_N	Analog IO	analog IO - clock RF RSSI
A11	Q_OUT2+	Analog IO	analog output+ IF_Q (channel 2)
B12	Q_OUT2-	Analog IO	analog output- IF_Q (channel 2)
A9	I_OUT2-	Analog IO	analog output- IF_I (channel 2)
B10	I_OUT2+	Analog IO	analog output+ IF_I (channel 2)
C11	AVDD12	Power 1.2 V	analog power 1.2v
B8	AVDD08	Power 0.8 V	analog power 0.8v
C9	AVDD18	Power 1.8 V	analog power 1.8v
A7	RX2_4	Analog IO	RF input 7G (channel 2)
A5	AVDD08	Power 0.8 V	analog power 0.8v
B6	RX2_3	Analog IO	RF input 5G (channel 2)
C7	AVDD12	Power 1.2 V	analog power 1.2v
A3	AVDD18	Power 1.8 V	analog power 1.8v
B4	RX2_2	Analog IO	RF input 3G (channel 2)
C5	AVDD08	Power 0.8 V	analog power 0.8v
D2	RX2_1	Analog IO	RF input 1G (channel 2)
C13	NC		
E29	NC		

4.2 SPI Interface

SPI interface pin descriptions that apply to the IceWings.

Table 4-2 SPI Pin description

Pin Name	Type	Description
SCK	Digital IO	SPI CLOCK
SS	Digital IO	SLAVE SELECT
MOSI	Digital IO	MASTER OUT SLAVE IN
MISO	Digital IO	MASTER IN SLAVE OUT

4.3 Supply and Ground Interface

Supply and Ground interface pin descriptions that apply to the IceWings.

Table 4-3 Supply and Ground Descriptions

Pin Name	Type	Description
AVDD12	Power	Analog Power 1.2 V
AVDD18	Power	Analog Power 1.8V
AVDD08	Ground	Analog Ground 0.8V
DVDD08	Power	Digital Power 0.8V
AVSS	Power	Digital Ground

5 System Specifications

5.1 Absolute Maximum Ratings

Table 5-1 Absolute Maximum Ratings

Parameter	Minimum	Maximum	Unit
Storage Temperature	-40	+150	°C
Operating Temperature (TA)	-40	+85	°C
Junction Temperature (T_j)	---	+125	°C
AVDD12	-0.3	1.32	V
AVDD18	-0.3	1.98	V
AVDD08	-0.3	0.88	V
DVDD08	-0.3	0.88	V

Note: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent device damage. These maximum ratings represent stress ratings only. Device operation at any maximum rating and/or above any condition indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

5.2 Crystal Specifications

Table 5-2 Crystal Specifications

Minimum	Default	Maximum	Tolerance	Unit
120	122.88	156.125	+/- 20ppm	MHz

5.3 ESD Specifications

Table 5-3 ESD Specifications

Symbol	Minimum	Maximum	Unit
EIA/JESD22_A114	-2,000	2,000	V
EIA/JESD22_A115	-200	200	V

5.4 Electrical Characteristics

Table 5-4 Electrical Characteristics

Parameter	Symbol	Mode	Min	Typ	Max	Unit
1.2V Analog Operating Voltage	AVDD12		1.14	1.2	1.26	V
1.8V Analog Operating Voltage	AVDD18		1.71	1.8	1.89	V
0.8V Analog Operating Voltage	AVDD08		0.72	0.8	0.88	V
0.8V Digital Operating Voltage	DVDD08		0.72	0.8	0.88	V
Input Low Voltage	V_{IL}		-0.30	0.0	0.4	V
Input High Voltage	V_{IH}		1.2	1.8	1.98	V
Operating VCTXO Frequency	F_{XTAL}		120	122.88	160	MHz

Table 5-5 Electrical Characteristics (IQ Interface)

Parameter	Symbol	Mode	Min	Typ	Max	Unit
IQ Output Common Mode Voltage	RX_IQ_O_CM		A: 0.7 B: 0.4	0.8	0.85	V
IQ Input Common Mode Voltage	TX_IQ_I_CM		0.2	0.6	A: 0.7 B: 1.0	V
IQ Output Swing (pp-diff)	RX_IQ_O_SW			1		Vpp
IQ Input Swing (pp-diff)	TX_IQ_I_SW			0.8	1	Vpp
IQ Output Load (Differential)	RX_IQ_LOAD		A: 800 B: 100			ohm

Table 5-6 VCTXO Typical phase noise Spec, 122.88MHz at 25 degrees Celsius

Frequency Offset	Phase Noise
1Hz offset	-45 dBc/Hz
10Hz offset	-75 dBc/Hz
100Hz offset	-100 dBc/Hz
1KHz offset	-122 dBc/Hz
10KHz offset	-141 dBc/Hz
100KHz offset	-146 dBc/Hz
1MHz offset	-147 dBc/Hz
5MHz offset	-152 dBc/Hz
20MHz offset	-162 dBc/Hz

Table 5-7 LVDS Driver

Parameter	Symbol	Mode	Min	Typ	Max	Unit
LVDS MAX Data rate	Fmax-LVDS	Transmit			800	Mb/s
Differential Output swing	SW_TX_LVDS	Transmit	250	350	400	mV
Output Common Mode Voltage	CM_TX_LVDS	Transmit	1.125	1.2	1.375	V
Propagation Delay	DEL_TX_LVDS	Transmit	125	150	250	ps

Table 5-8 LVDS Receiver

Parameter	Symbol	Mode	Min	Typ	Max	Unit
LVDS MAX Data rate	Fmax-LVDS	Receive			800	Mb/s
Differential Input Swing	SW_RX_LVDS	Receive	200		600	mV
Receiver Differential Impedance	RX_TERM_LVDS	Receive	90	100	110	ohm
Receiver Common Mode	RX_CM_LVDS	Receive	0.4		1.5	V

Table 5-9 Fast Power down GPIOs

GPIO Name	Boolean	Chip Status
RX_OFF	0	All RX Paths are ON
	1	All RX Paths are OFF, Synthesizers are ON. Clock Gen is ON
TX_OFF	0	All TX paths are ON
	1	All TX Paths are OFF, Synthesizers are ON. Clock Gen is ON

6 SPI Timing Specifications

7.1 Overview

This section provides a brief description of IceWings SPI interface and implemented READ/WRITE command and frame structure.

6.1.1 Register Structure

A register file with 32-bit registers is used. For example, the first register can have a 0x00 hex address, the next would be 0x01, and so on.

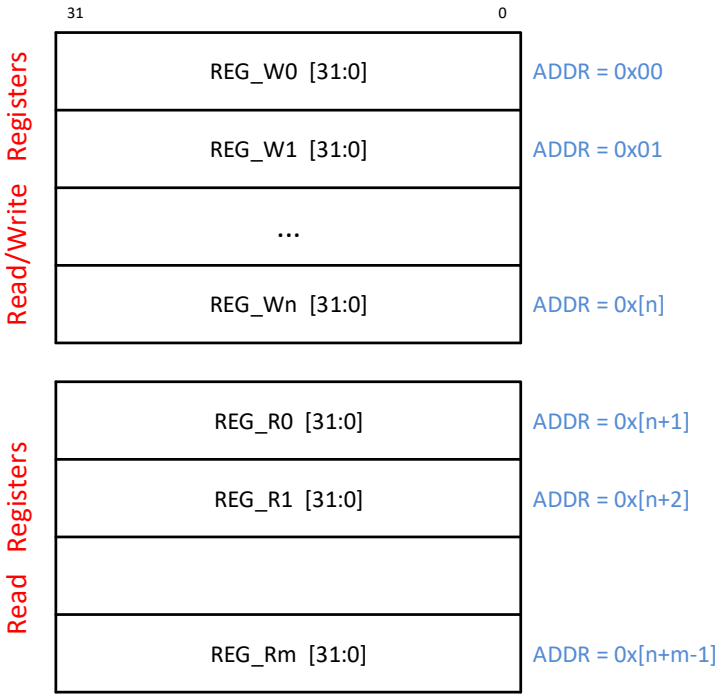


Figure 6-1 Register File

6.1.2 WRITE/READ Frame Structure

The READ/WRITE frame structure is depicted in the following figures. As shown in Figure 7-2, the SPI Master sends MOSI data on the RISING EDGE of SCLK while on IceWings chip side, MOSI data is latched on the FALLING EDGE of the SCK clock.

For the MISO signal, data will be sent on the RISING EDGE of SCK from IceWings chip side while on the SPI Master side, MISO data is latched on FALLING EDGE of SCK.

Master and slave both should send the data on rising edge of the SCK and sample the data on SCK falling edge. In other words, every TX operation for sending the data (Both on slave and master) should be on the rising edge of the SCK and any RX operation for sampling the data should be on the

falling edge of the SCK. Setting CPHA mode = 1 and CPOL mode = 0 would configure the SPI structure to the desired format.

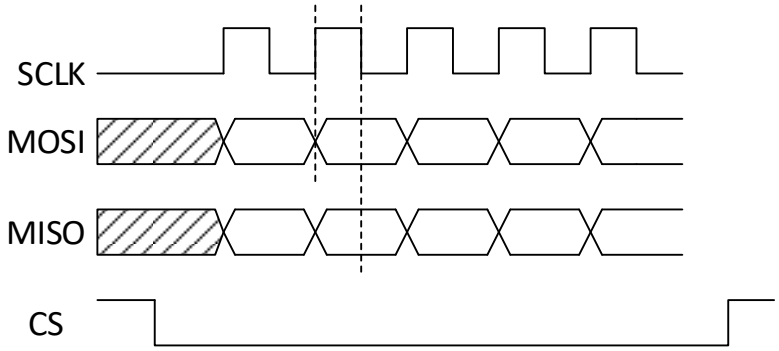


Figure 6-2 MOSI/MISO Timing

The total Write command frame length is 6 bytes. The first two bytes indicate one bit W/Rb following with 15 bits of address then four bytes of Write/Read of the 32-bit register. The data is sent/received as MSB first.

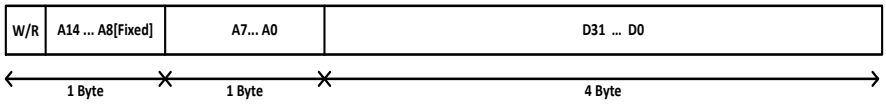


Figure 6-3 SPI Frame Structure

6.1.3 Frame Address/Data Structure

The W/Rb bit is the first sent bit on MOSI from the SPI Master side. The ONE on this bit starts a WRITE operation command and a ZERO means a READ command start.

The next 15bits on a frame after the W/Rb bit are address bits. Since the IP core supports both SPI/I2C, the address scheme has two parts. The first 7 bits of the SPI address is a 7-bit fixed address and it is equal to 7 bits of the I2C slave address, for example 0xC2. The next 8 bits of address are the regular register address, which varies from 0 to 255 for each 32-bit register.

Following the 1-bit W/Rb and 15-bit address, the 32 bits of data will be sent on MOSI on a WRITE operation by the SPI Master, or on MISO in READ operation by the IceWings chip.

6.1.4 WRITE, Sample Frame for SPI

Figure 7-4 depicts a sample WRITE command of SPI. As shown, two bytes of address including one byte I2C address and one byte of register address following with 4 bytes of data were sent on the MOSI port with MSB first order by the SPI Master device. The Master should drive SCK for every single bit on MOSI. As an example, shown in Figure 7-4, the 32 bits data of 0xF0F0F0F0 hex have been written in the I2C address of 0xC0 and register address of 0x10.

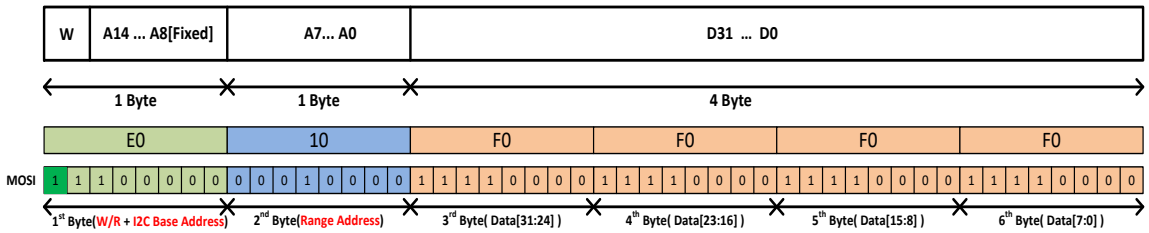


Figure 6-4 SPI WRITE Command Frame

6.1.5 READ, Sample Frame for SPI

To read a 32-bit register from the register address of 0x10, the Master needs to send 0x60 as first sent byte on MOSI following with 0x10 as the register address. Then the Master should apply 32 SCK clock to shift-out the 32-bit READ data on MISO.

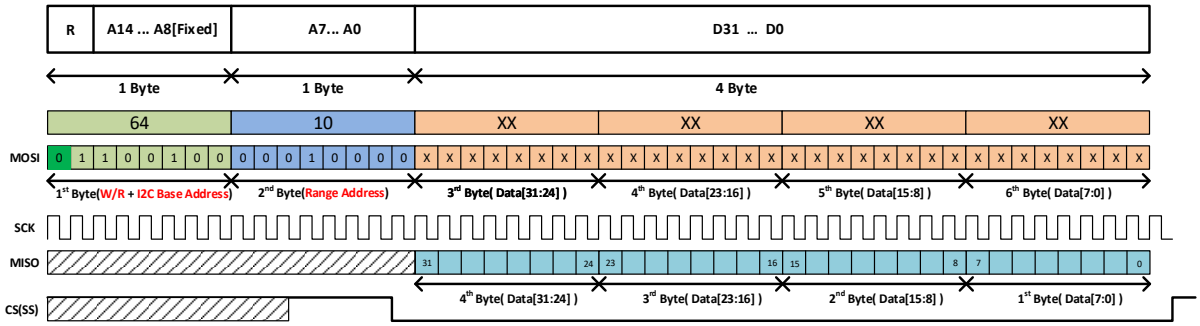
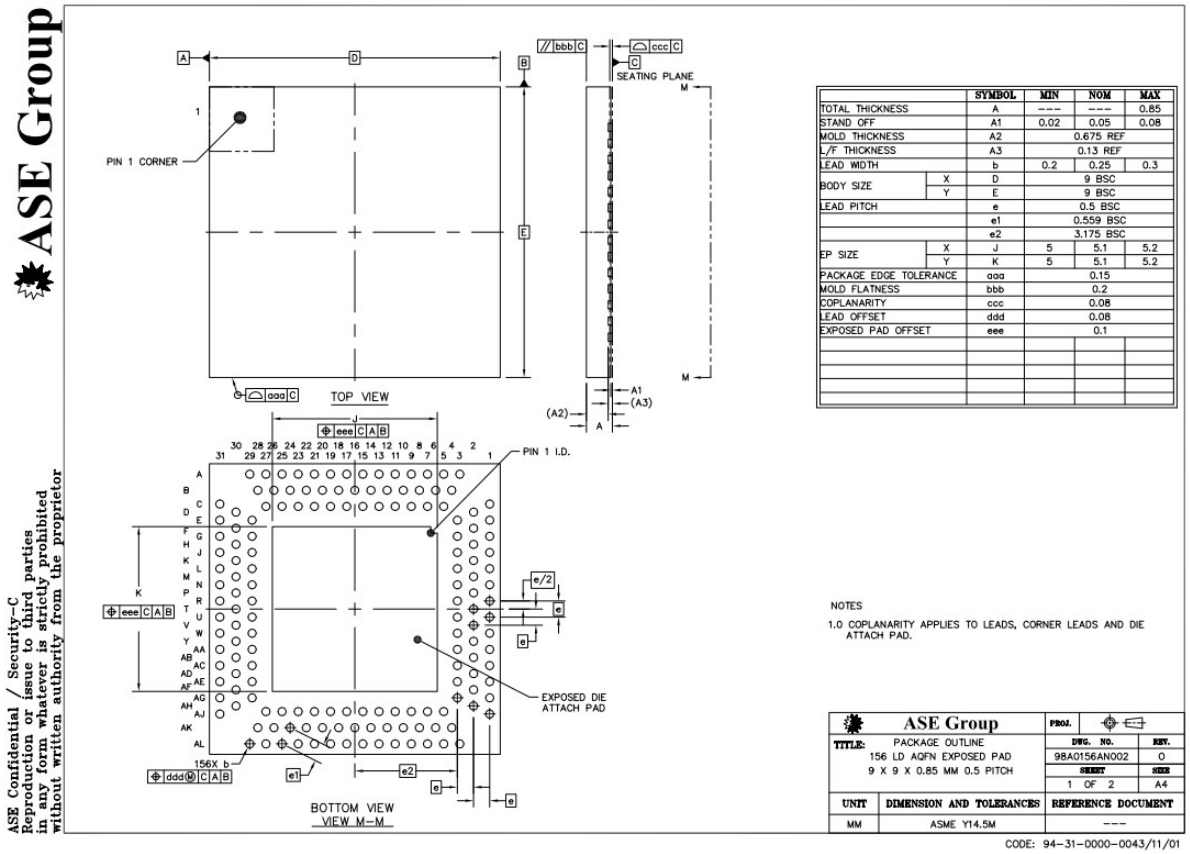


Figure 6-5 SPI READ Command Frame

7 Package Information

7.1 STNA504 Package Information



		SYMBOL	MIN	NOM	MAX
TOTAL THICKNESS		A	---	---	0.85
STAND OFF		A1	0.02	0.05	0.08
MOLD THICKNESS		A2		0.675 REF	
L/F THICKNESS		A3		0.13 REF	
LEAD WIDTH		b	0.2	0.25	0.3
BODY SIZE	X	D		9 BSC	
	Y	E		9 BSC	
LEAD PITCH		e		0.5 BSC	
		e1		0.559 BSC	
		e2		3.175 BSC	
EP SIZE	X	J	5	5.1	5.2
	Y	K	5	5.1	5.2
PACKAGE EDGE TOLERANCE		aaa		0.15	
MOLD FLATNESS		bbb		0.2	
COPLANARITY		ccc		0.08	
LEAD OFFSET		ddd		0.08	
EXPOSED PAD OFFSET		eee		0.1	

Figure 7-1 Package

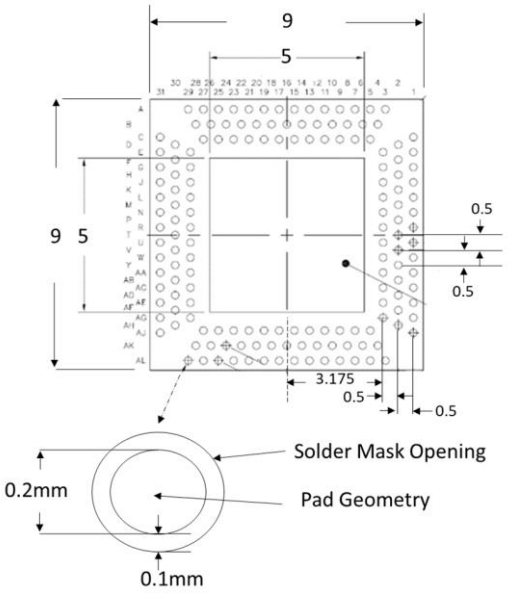


Figure 7-2 Package footprint

7.2 Thermal Resistance

The package's thermal performance is represented by the parameters shown in Table 8-1.

Table 7-1 Package Thermal Performance

Parameter	Definition	Calculation	Description
Θ_{JA}	Thermal resistance from junction to ambient	$\Theta_{JA} = (T_J - T_A) / P_H$	Where: T_J is the Junction Temperature, T_A is the Ambient Temperature, P_H is the Power Dissipation Θ_{JA} represents the resistance to the heat flows from the chip to ambient air. It is an index of heat dissipation capability. Lower Θ_{JA} means better thermal performance.

Theta ja (C/ W)			Psi jt (C/W)	Theta jc (C/W)	Theta jb (C/W)
0 m/s	1 m/s	2 m/s			
23.1	20.0	19.0	0.22	8.6	10.50

7.3 Green Technology in Packaging

All ICs from Arctic are fully compliant with RoHS 2.0 Restriction of the Use of Certain Hazardous Substances in Electrical and Electronic Equipment (EU) 2015/863 and its amendment, which apply to the Removal of Harmful Substances, including materials listed in Table 8-2:

Table 7-2 Removal of Hazardous Substances (RoHS)

Symbol	Material	Maximum
Pb	Lead and its compounds	< 1,000 ppm
Hg	Mercury and its compounds	< 1,000 ppm
Cd	Cadmium and its compounds	< 100 ppm
Cr+6	Hexavalent chromium compounds	< 1,000 ppm
PBB	Polybrominated Biphenyls	< 1,000 ppm
PBDE	Polybrominated Diphenylethers	< 1,000 ppm
DEHP	Bis (2-Ethylhexyl) C	< 1,000 ppm
BBP	Benzyl Butyl Phthalate	< 1,000 ppm
DBP	Dibutyl Phthalate	< 1,000 ppm
DIBP	Diisobutyl Phthalate	< 1,000 ppm

Arctic currently offers lead(Pb)-free ICs (devices ordered and marked with an "1" suffix); they contain no harmful substances beyond levels specified in Sony Technical Standard SS-00259-1. In addition, all Arctic ICs marked with a "2" suffix are Green packages that meet or exceed stringent

requirements to reduce harmful substances specified in Sony Technical Standard SS-00259-1 and in various EU Directives. This includes all of the RoHS materials listed in All ICs from Arctic are fully compliant with RoHS 2.0 Restriction of the Use of Certain Hazardous Substances in Electrical and Electronic Equipment (EU) 2015/863 and its amendment, which apply to the Removal of Harmful Substances, including materials listed in Table 8-2:

Table 7-2 Removal of Hazardous Substances (RoHS)

8-3 plus those listed:

No EU REACH Substance of Very High Concern (SVHC) is used in the manufacture of Arctic's products. Arctic ICs used in consumer products continue to enhance the visual enjoyment of viewers, as well as lessen the impact of substances on the ecosystem and protect our planet.

7.4 Moisture Sensitivity Level

The usual shipping process for Arctic chips includes handling and dry packing the product in accordance with the following standards:

- IPC/JEDEC J-STD-020, *Moisture/Reflow Sensitivity Classification for Nonhermetic Solid State Surface Mount Devices*: Classifies devices that are sensitive to moisture-induced stress.

- IPC/JEDEC J-STD-033, *Handling, Packing, Shipping and Use of Moisture/Reflow Sensitive Surface Mount Devices*: Provides standardized methods for handling, packing, shipping, and use of moisture/reflow sensitive SMD packages to avoid damage and provide a minimum shelf life.

More detailed information about these standards can be found at http://www.jedec.org/ (the Standards Resource for the World Semiconductor Industry).

Note:

Arctic ICs are classified as Moisture Sensitivity Level (MSL) 3.

MSL 3 has a floor life of 168 hours at ≤ 30 ˚C / 60% RH (relative humidity). The following is an overview of the process to qualify chips at this level; please refer to the corresponding JEDEC standards for more detailed information.

1**. Begin with:**

a. External visual inspection

b. Electrical test

c. Acoustic microscopy

2. **Bake:** 24 hours at 125 +5/-0 ˚C

3. **Moisture Soak:** 192 hours at 30 ˚C / 60% RH (relative humidity)

4. **Reflow:** Subject the sample to a maximum of three cycles of the appropriate reflow conditions

5**. Perform:**

a. Final external visual inspection

b. Final electrical test

c. Final acoustic microscopy

Upon receipt of the product, customers should inspect the condition of the Moisture Barrier Bags and Humidity Indicator Cards, in accordance with the IPC/JEDEC J-STD-033 standard

7.5 Sample Reflow Profiles

Table 8-3 lists the classification reflow profiles.

Table 7-3 Classification Reflow Profiles

Profile Feature	**Pb Free / Green Assembly**
Preheat / Soak Temperature Min (Tsmin) Temperature Max (Tsmax) Time (t_s) from (Tsmin to Tsmax)	 150˚C 200˚C 60 ~ 120 seconds
Ramp-up rate (T_L to T_p)	3˚C/second max.
Liquidous temperature (T_L) Time (t_L) maintained above T_L	217˚C 60 ~ 150 seconds
Peak package body temperature (T_p)	260˚C
Time (t_p)* within 5 ˚C of the specified classification temperature (T_c)	30* seconds
Ramp-down rate (T_p to T_L)	6˚C/second max.
Time 25˚C to peak temperature	8 minutes max.

* Tolerance for peak profile temperature (T_p) is defined as a supplier minimum and a user maximum.

Notes:

1. All temperatures refer to the center of the package, measured on the package body surface that is facing up during assembly reflow (e.g., live-bug). If parts are reflowed in other than the normal live-bug assembly reflow orientation (i.e., dead-bug), T_p shall be within +/- 2˚C of the live-bug T_p and still meet the T_c requirements, otherwise, the profile shall be adjusted to achieve the latter. To accurately measure actual peak package body temperatures, refer to JEP140 for recommended thermocouple use.

2. Reflow profiles in this document are for classification/preconditioning and are not meant to specify board assembly profiles. Actual board assembly profiles should be developed based on specific process needs and board designs and should not exceed the parameters in Table 5-12.

- For example, if Tc is 260˚C and time t_p is 30 seconds, this means the following for the supplier and the user.
  - For a user: The peak temperature must not exceed 260˚C. The time above 255˚C must not exceed 30 seconds.
  - For a supplier: The peak temperature must be at least 260˚C. The time above 255˚C must be at least 30 seconds.

3. Maximum of 3 reflows

Figure 8-3 shows a sample reflow profile for a green package. To achieve optimum reflow, the profile values f

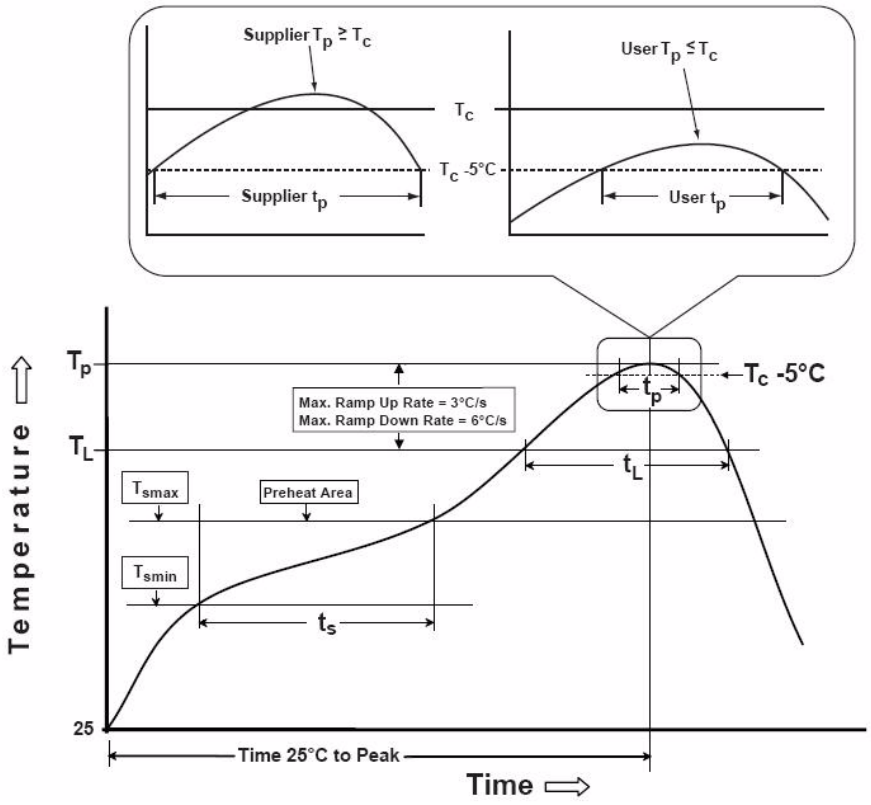


Figure 7-3 Reflow Profile—Green Package

or your design may need to be adjusted.

7.6 Package Topside Marking

Figure 7-4 Package Topside Marking

Table 8-5 Package Topside Marking Explanation

Mark Method	Laser	
Line 1	Pin 1 Identifier	Circle = Top, Left
Line 2	IC Manufacturer	ARCTIC or logo
Line 3	Family Name, Part Number, Device Version	STNA504-M1
Line 4	Temperature Range, Package Pins, Package Type, Package Finish, Product Status	L-156-QN1
Line 5	Datecode (YYWW) Device Assembled	DC2230

8 Test Report

8.1 Transmit Tests

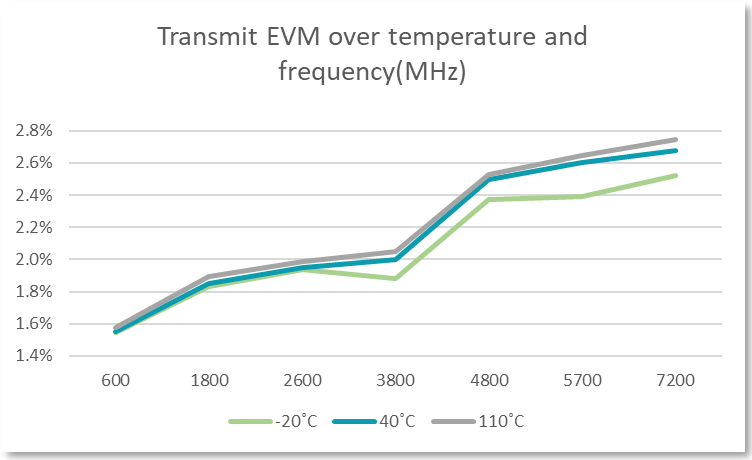


Figure 5 Transmit EVM over temperature and frequency for a 100MHz 5G NR waveform with CS= 30kHz and 256QAM

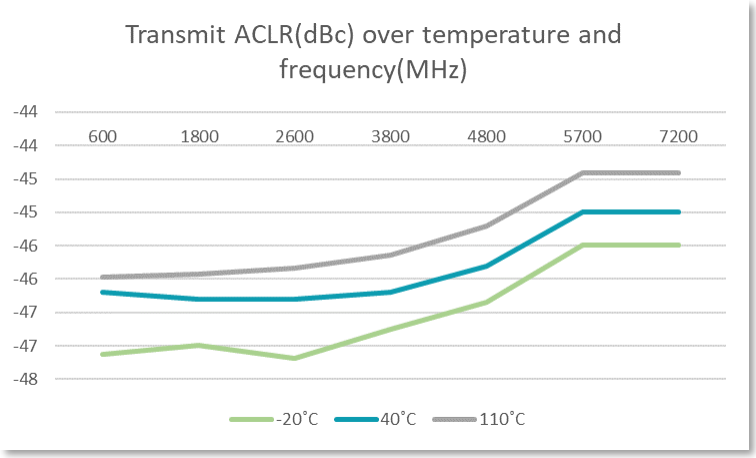


Figure 6 Transmit ACLR over temperature and frequency for a 100MHz 5G NR waveform with CS= 30kHz and 256QAM

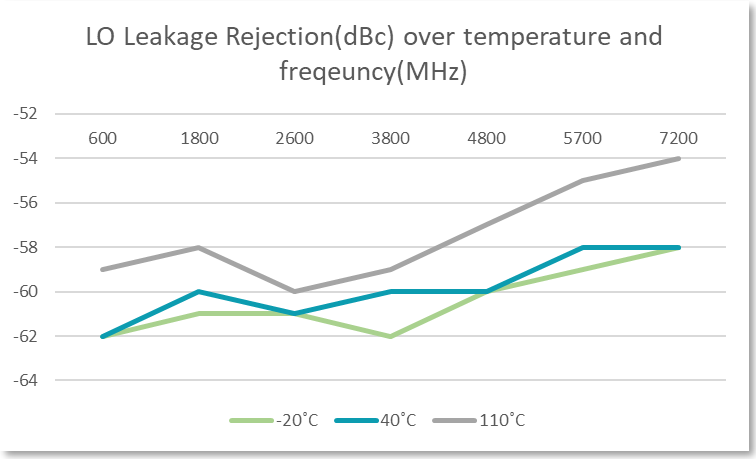


Figure 7 Transmit LO leakage over temperature and frequency for a 100MHz 5G NR waveform with CS= 30kHz and 256QAM

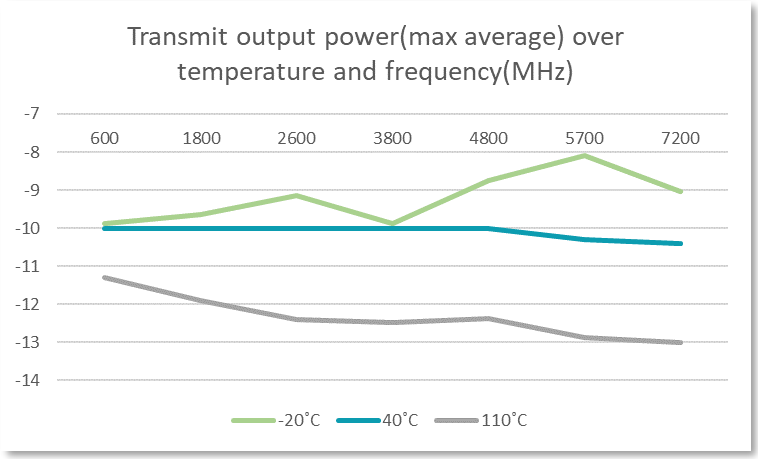


Figure 8 Transmit output power over temperature and frequency for a 100MHz 5G NR waveform with CS= 30kHz and 256QAM

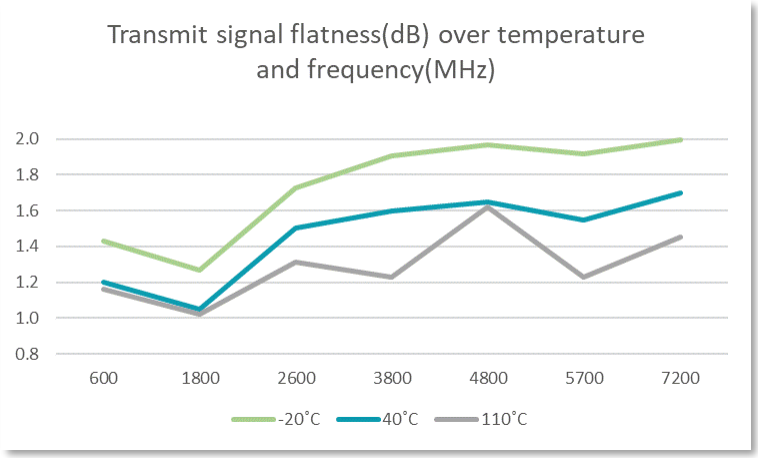


Figure 9 Transmit signal flatness over temperature and frequency for a 100MHz 5G NR waveform with CS= 30kHz and 256QAM

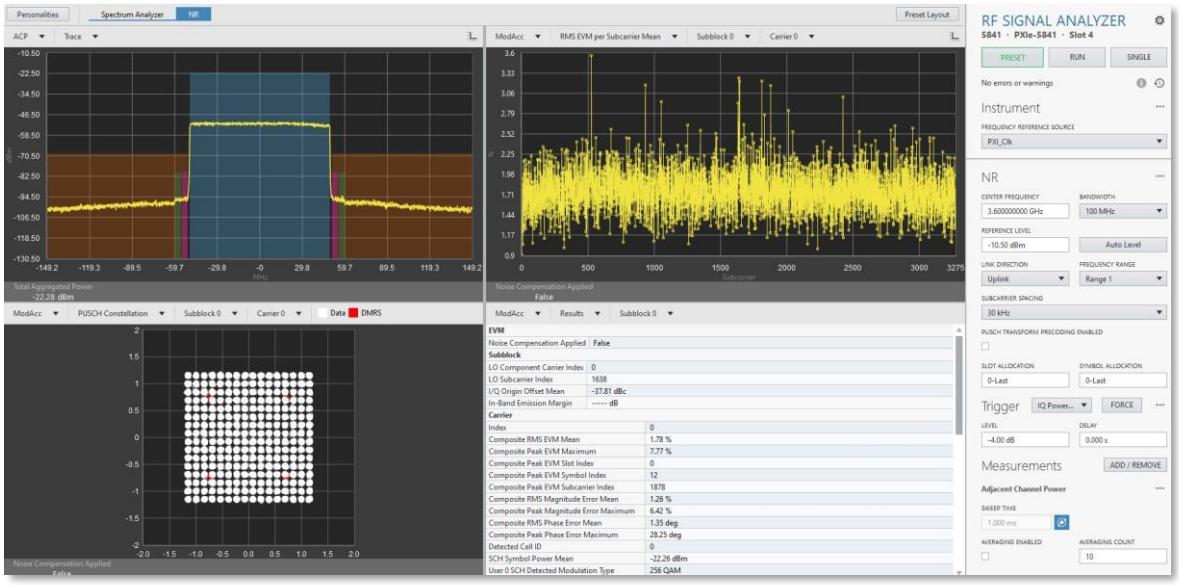


Figure 10 Transmit constellation at for 100MHz 5G NR waveform with CS= 30kHz and 256QAM at 3.6GHz LO frequency with EVM of 1.78%

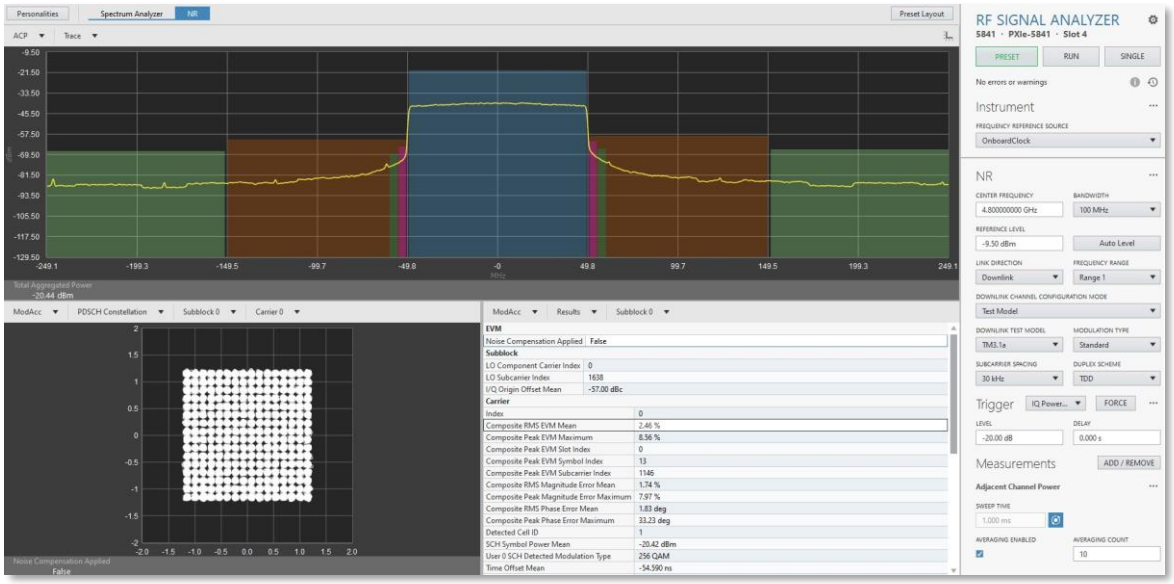


Figure 11 Transmit constellation at for 100MHz 5G NR waveform with CS= 30kHz and 256QAM at 4.8GHz LO frequency with EVM of 2.46%

8.2 Receive Tests

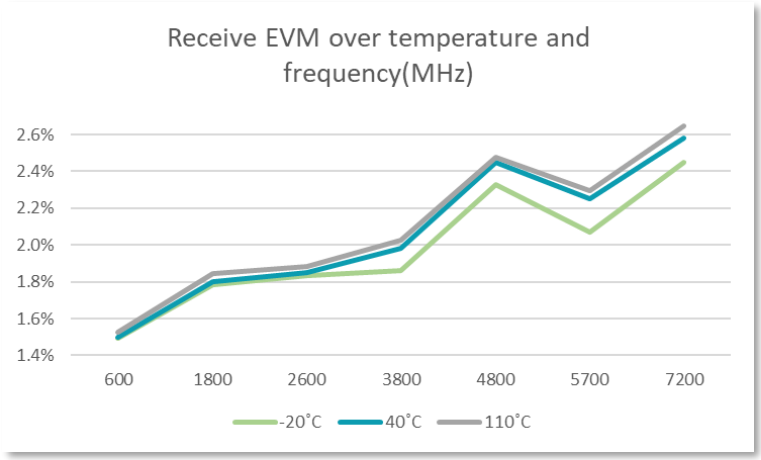


Figure 12 Receive EVM over temperature and frequency for a 100MHz 5G NR waveform with CS= 30kHz and 256QAM

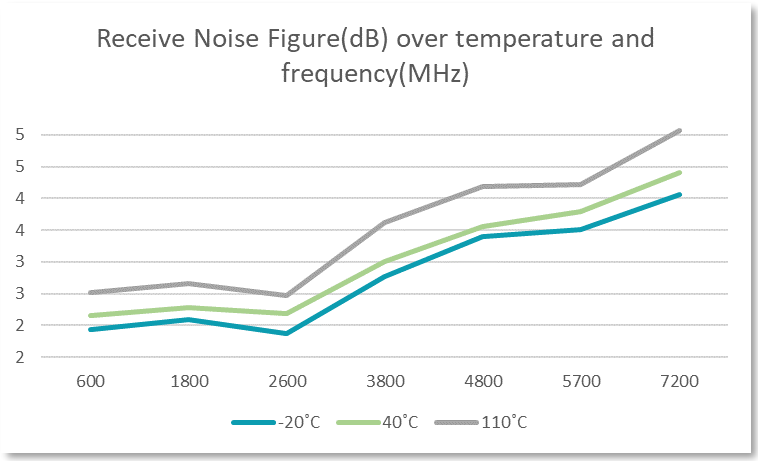


Figure 13 Receive Noise Figure over temperature and frequency for a 100MHz 5G NR waveform with CS= 30kHz and 256QAM

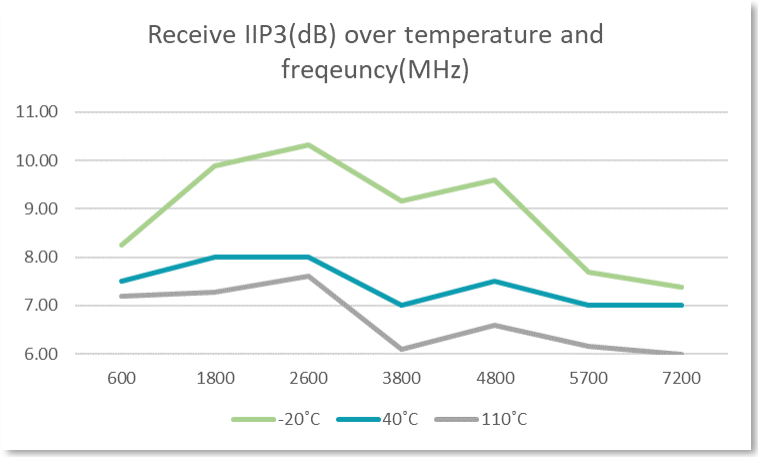


Figure 14 Receive IIP3 over temperature and frequency for a 100MHz 5G NR waveform with CS= 30kHz and 256QAM

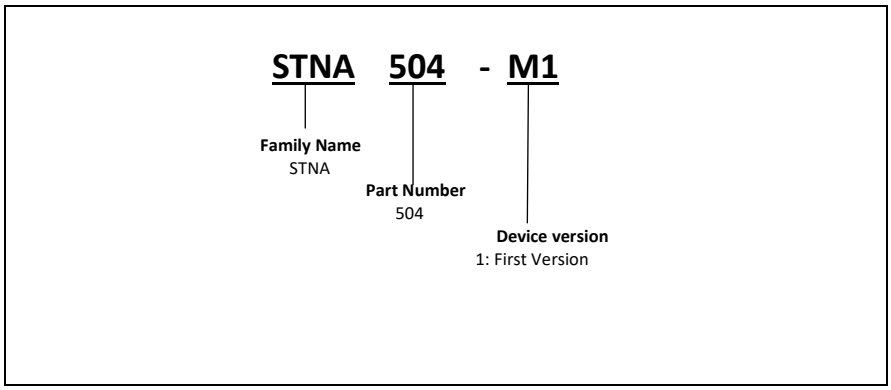
9 Ordering Information

9.1 Ordering Part Number

Table 9-1 Ordering Part Number

Part Number	Product Type	Package Dimension	Lead Free	Shipping Format
STNA504-M1	156 pin QFN	9 x 9 x 0.85 mm	Yes	Tape & Reel

9.2 Part Number Definitions



Notes:

1. * The 1st Device Version character represents a Major Change (changed only with structural or functional changes in the die)
2. **The 2nd Device Version character represents a Minor Change (the change made is not structural or functional)
3. *** Package dimensions for the 156-pin QFN are mm.

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10 Revision History

Table 10-1 Revision History

Datasheet Version	Release Date	Changes	Modified Sections
IceWings STNA504	Initial release Sept 2022	-	-
IceWings STNA504-M1	Oct' 2022	Update Part Number	Page 39, 40
IceWings STNA504-M1	Dec'2022	Update package to device version, current consumption	Page 41, 13
IceWings STNA504-M1	March'2023	Company name/ Logo	
IceWings STNA504-M1	April'2023	Add package thermal data	Page 35